AMENDMENTS TO THE CLAIMS

Claims 1-38. (Canceled)

39. (Original) A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming at least one isolation region in a substrate;

forming a gate of a transistor over said substrate, said gate being spaced apart from said at least one isolation region;

forming a first doped layer of a first conductivity type in said substrate;

forming a doped region of a second conductivity type in said doped layer; and

forming a second doped layer of said first conductivity type in said substrate by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle in an area of said substrate defined between said gate and said at least one isolation region, said gate acting as an implant mask for said incidence angle, said second doped layer being in contact with said isolation region and being displaced laterally from an electrically active portion of said gate by a distance.

40. (Original) The method of claim 39, wherein said second doped layer is laterally displaced from said electrically active portion of said gate by about 100 to about 2,500 Angstroms.

41. (Original) The method of claim 39, wherein said second doped layer is laterally displaced from said electrically active portion of said gate by about 200 to about 1,000 Angstroms.

42. (Original) The method of claim 39, wherein said first conductivity type is p-type and said second conductivity type is n-type.

43. (Original) The method of claim 39, wherein said act of forming said doped region of said second conductivity type further comprises forming a photoresist layer over said substrate and said gate, and patterning said photoresist layer to expose said area of said substrate located between said gate and said at least one isolation region.

44. (Original) The method of claim 43, wherein said angle of said implanting is of about 3 degrees to about 40 degrees.

45. (Original) The method of claim 44, wherein the height of said gate is of about 400 Angstroms to about 4,000 Angstroms and the thickness of said photoresist layer is of about 1,000 Angstroms to about 10,000 Angstroms.

46. (Original) The method of claim 39, wherein said act of implanting ions of said first conductivity type further comprises directing a dopant at said incidence angle which is different than a zero degree angle in said area of said substrate located between said gate and said at least one isolation region.

47. (Original) The method of claim 39, wherein said photodiode is formed as a p-n-p photodiode.

48. (Original) A method of forming a p-n-p photodiode for a CMOS imaging device, said method comprising:

forming at least one field oxide region in a silicon substrate;

forming a transistor gate over said silicon substrate and spaced apart from said at least one field oxide region;

forming an n-type doped region in said silicon substrate by implanting n-type ions at an incidence angle with said silicon substrate other than ninety degrees;

forming an insulating layer over said transistor gate and said silicon substrate; and

forming a p-type doped layer within said silicon substrate and above said n-type doped region, said p-type doped layer being in contact with said isolation region and being displaced laterally from an electrically active area of said transistor gate by a distance, said p-type doped layer having a dopant concentration within the range of from about 1×10^{17} to about 1×10^{19} atoms per cm^3.

49. (Original) The method of claim 48, wherein said p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 100 to about 2,500 Angstroms.

50. (Original) The method of claim 48, wherein said p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 200 to about 1,000 Angstroms.

51. (Original) The method of claim 48, wherein said act of forming said p-type doped layer further comprises implanting p-type ions at an incidence angle with said silicon substrate other than zero degrees.

52. (Original) The method of claim 48, wherein said act of forming said p-type doped layer further comprises implanting p-type ions at an incidence angle with said silicon substrate of about zero degrees.

53. (Original) The method of claim 48, wherein said act of forming said n-type doped region further comprises forming a photoresist layer over said silicon substrate and said gate.

54. (Original) The method of claim 53, wherein said act of forming said n-type doped region further comprises patterning said photoresist layer to expose an area of said silicon substrate located between said transistor gate and said at least one isolation region.

55. (Original) The method of claim 54, wherein said photoresist layer is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms.

56. (Original) The method of claim 55, wherein said implanting act is conducted at an angle of about 3 degrees to about 40 degrees.

57. (Original) The method of claim 56, wherein the height of said transistor gate is of about 400 Angstroms to about 4,000 Angstroms.

58. (Original) The method of claim 48, wherein said n-type doped region has a dopant concentration within the range of from about 1×10^{16} to about 5×10^{17} atoms per cm^3.

59. (Original) A method of forming a p-n-p photodiode for a pixel sensor cell, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate over said substrate and spaced apart from said at least one field oxide region;

forming a first p-type doped layer in said substrate;

forming a photoresist layer over said transistor gate and said field oxide region;

patterning said photoresist layer to form an opening extending between a first location and a second location, said first location corresponding to a first point over said transistor gate and said second location corresponding to a second point over said field oxide region;

conducting a first implant through said opening to form an n-type doped region in said first p-type doped layer; and

conducting an angled implant through said opening to form a second p-type doped layer in said first p-type doped layer, said second p-type doped

layer being located above said n-type doped region and laterally spaced thereof at a surface region of said substrate.

60. (Original) The method of claim 59, wherein said second p-type doped layer is formed in contact with said isolation region.

61. (Original) The method of claim 59, wherein said second p-type doped layer is displaced laterally from an electrically active area of said transistor gate by a distance.

62. (Original) The method of claim 59, wherein said second p-type doped layer is laterally displaced from said electrically active area of said transistor gate by about 100 to about 2,500 Angstroms.

63. (Original) The method of claim 59, wherein said second p-type doped layer has a dopant concentration within the range of from about 1 x 10^{17} to about 1 x 10^{19} atoms per cm^3.

64. (Original) The method of claim 59, wherein said photoresist layer is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms.

65. (Original) The method of claim 64, wherein said angle of said angled implant is of about 3 degrees to about 40 degrees.

66. (Original) The method of claim 65, wherein the height of said transistor gate is of about 400 Angstroms to about 4,000 Angstroms.

67. (Original) A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming at least one isolation region in a substrate of a first conductivity type;

forming a gate of a transistor over said substrate, said gate being spaced apart from said at least one isolation region;

conducting a first angled implant to form a doped region of a second conductivity type in said substrate; and

conducting a second angled implant to form a doped layer of said first conductivity type in said substrate by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle in an area of said substrate defined between said gate and said at least one isolation region, said gate acting as an implant mask for said incidence angle, said doped layer being in contact with said isolation region and being displaced laterally from an electrically active portion of said gate by about 100 to about 2,500 Angstroms.

68. (Original) The method of claim 67, wherein said doped layer is laterally displaced from said electrically active portion of said gate by about 200 to about 1,000 Angstroms.

69. (Original) The method of claim 67, wherein said act of conducting said second angled implant further comprises forming a photoresist layer over said substrate and said gate, and patterning said photoresist layer to expose said area of said substrate located between said gate and said at least one isolation region.

70. (Original) The method of claim 69, wherein said act of conducting said second angled implant further comprises directing ions of said first conductivity type at an incidence angle with said substrate which is different than a ninety degree angle in said area of said substrate located between said gate and said at least one isolation region.

71. (Original) The method of claim 70, wherein said incidence angle is of about 3 degrees to about 40 degrees.

72. (Original) The method of claim 71, wherein the height of said gate is of about 400 Angstroms to about 4,000 Angstroms and the thickness of said photoresist layer is of about 1,000 Angstroms to about 10,000 Angstroms.

73. (Original) The method of claim 67, wherein said act of conducting said first angled implant further comprises directing ions of said second conductivity type at an incidence angle with said substrate which is different than a zero degree angle.

74. (New) A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming at least one isolation region in a substrate;

forming a gate of a transistor over said substrate, said gate being spaced apart from said at least one isolation region;

forming a first doped layer of a first conductivity type in said substrate;

forming a doped region of a second conductivity type in said doped layer; and

forming a second doped layer of said first conductivity type in said substrate by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle in an area of said substrate defined between said gate and said at least one isolation region, said second doped layer being in contact with said isolation region and being displaced laterally from an electrically active portion of said gate by a distance.